

AMENDMENTS TO CLAIMS

In light of the election of elects Group I (*i.e.* claims 1 - 8 and 21 - 24), this will replace all prior listings of claims in the application:

Listing of Claims:

1. (Original) A semiconductor device, comprising:
a substrate;
a dielectric layer formed over the substrate;
a damascene interconnect structure defined in the dielectric layer; and
a barrier layer deposited over the dielectric layer and within the
damascene interconnect structure, the barrier layer within the
damascene interconnect structure being tapered.
2. (Original) A semiconductor device as recited in claim 1, wherein the
barrier layer is tapered within the damascene interconnect structure so the
barrier layer is thinner toward an edge of the damascene interconnect
structure and thicker toward a bottom portion of the damascene interconnect
structure.
3. (Original) A semiconductor device as recited in claim 1, wherein the
damascene interconnect structure is one of a via and a trench.
4. (Original) A semiconductor device as recited in claim 1, further
comprising:
a copper layer formed over the barrier layer and filling the damascene
interconnect structure; and
a cap layer deposited over the copper layer and the barrier layer.
5. (Original) A semiconductor device as recited in claim 1, wherein the
barrier layer is made from at least one of Ta, W, Ru, Rh, Co, and Ni.

6. (Original) A semiconductor device as recited in claim 1, wherein the barrier layer is between 100 Angstroms to 500 Angstroms in thickness.
7. (Original) A semiconductor device as recited in claim 1, wherein the barrier layer is between 200 Angstroms and 250 Angstroms in thickness.
8. (Original) A semiconductor device as recited in claim 1, wherein the dielectric layer is one of a silicon dioxide and a low-k dielectric.
9. (Withdrawn) A method for making a semiconductor device, comprising:
 - providing a substrate;
 - forming a dielectric layer over the substrate;
 - defining a damascene interconnect structure in the dielectric layer; and
 - forming a barrier layer over the dielectric layer and within the damascene interconnect structure, the barrier layer being tapered within the damascene interconnect structure.
10. (Withdrawn) A method for making a semiconductor device as recited in claim 9, wherein defining the damascene interconnect structure includes defining one of a via and a trench.
11. (Withdrawn) A method for making a semiconductor device as recited in claim 9, further comprising:
 - depositing a metal layer over the dielectric layer and the damascene interconnect structure;
 - planarizing the metal layer; and
 - applying a cap layer over the planarized metal layer and the barrier layer.

12. (Withdrawn) A method for making a semiconductor device as recited in claim 9, wherein forming a barrier layer over the dielectric layer and within the damascene interconnect structure includes, depositing a barrier layer over the dielectric layer and within the damascene interconnect structure; and plasma etching the barrier layer while applying a voltage to the substrate, the voltage being a negative potential.

13. (Withdrawn) A method for making a semiconductor device as recited in claim 9, wherein forming a barrier layer over the dielectric layer and within the damascene interconnect structure includes, depositing a barrier layer over the dielectric layer and within the damascene interconnect structure; and electrochemically etching the barrier layer while applying a voltage to the substrate, the voltage being a positive potential.

14. (Withdrawn) A method for making a semiconductor device as recited in claim 9, wherein forming the barrier layer includes applying a voltage to the substrate through a substrate holder during an etching operation.

15. (Withdrawn) A method for making a semiconductor device as recited in claim 9, wherein the method further includes forming the barrier layer using at least one of Ta, W, Ru, Rh, Co, and Ni.

16. (Withdrawn) A semiconductor device as recited in claim 9, wherein the method further includes forming the barrier layer between 100 Angstroms to about 500 Angstroms in thickness.

17. (Withdrawn) A method for making a semiconductor device as recited in claim 9, further comprising:

depositing a copper seed layer over the dielectric layer and within the damascene interconnect structure;
depositing a copper layer over the copper seed layer to fill the damascene interconnect structure;
planarizing the copper layer; and
applying a cap layer over the planarized copper layer and the barrier layer.

18. (Withdrawn) A method for making a semiconductor device, comprising:

providing a substrate;

forming a dielectric layer over the substrate;

defining one of a via and a trench in the dielectric layer;

depositing a barrier layer over the dielectric layer and within the damascene interconnect structure; and

etching the barrier layer while applying a voltage to the substrate, the etching generating a tapered barrier layer within the damascene interconnect structure.

19. (Withdrawn) A method for making a semiconductor device as recited in claim 18, wherein the etching is a plasma etching and the voltage applied is a negative potential.

20. (Withdrawn) A method for making a semiconductor device as recited in claim 18, wherein the etching is a chemical etching and the voltage applied is a positive potential.

21. (Original) A system with a damascene interconnect structure, comprising:

a microprocessor including a damascene interconnect structure with a tapered barrier layer within the damascene interconnect structure;
a bus coupled to the microprocessor; and
a network interface coupled to the bus.

22. (Original) A system with a damascene interconnect structure as recited in claim 21, wherein the tapered barrier layer is generated by application of a voltage to the damascene interconnect structure during etching of the barrier.

23. (Original) A system with a damascene interconnect structure as recited in claim 22, wherein the etching includes one of a plasma etching and an electrochemical etching.

24. (Original) A system with a damascene interconnect structure as recited in claim 23, wherein a negative potential is applied when the plasma etching is used and a positive potential is applied when the electrochemical etching is used.